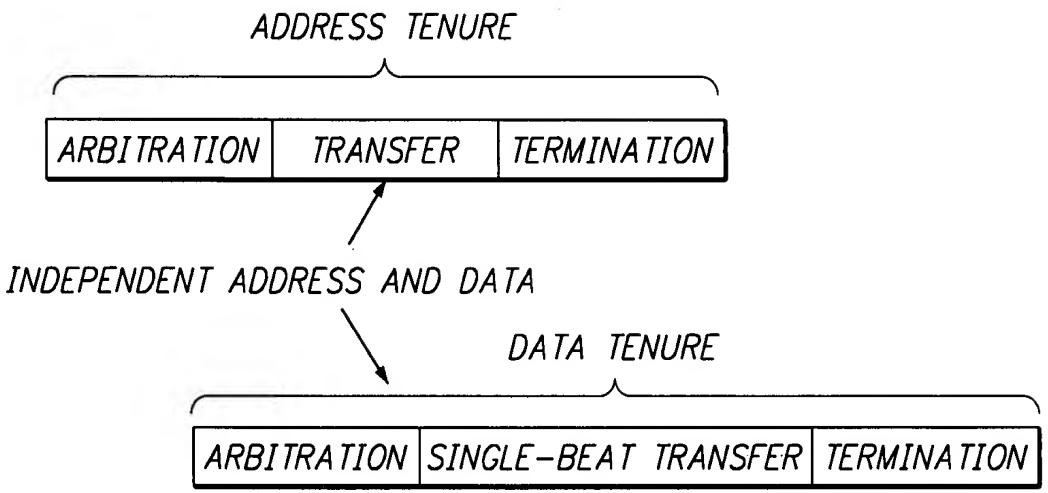


FIG. 1

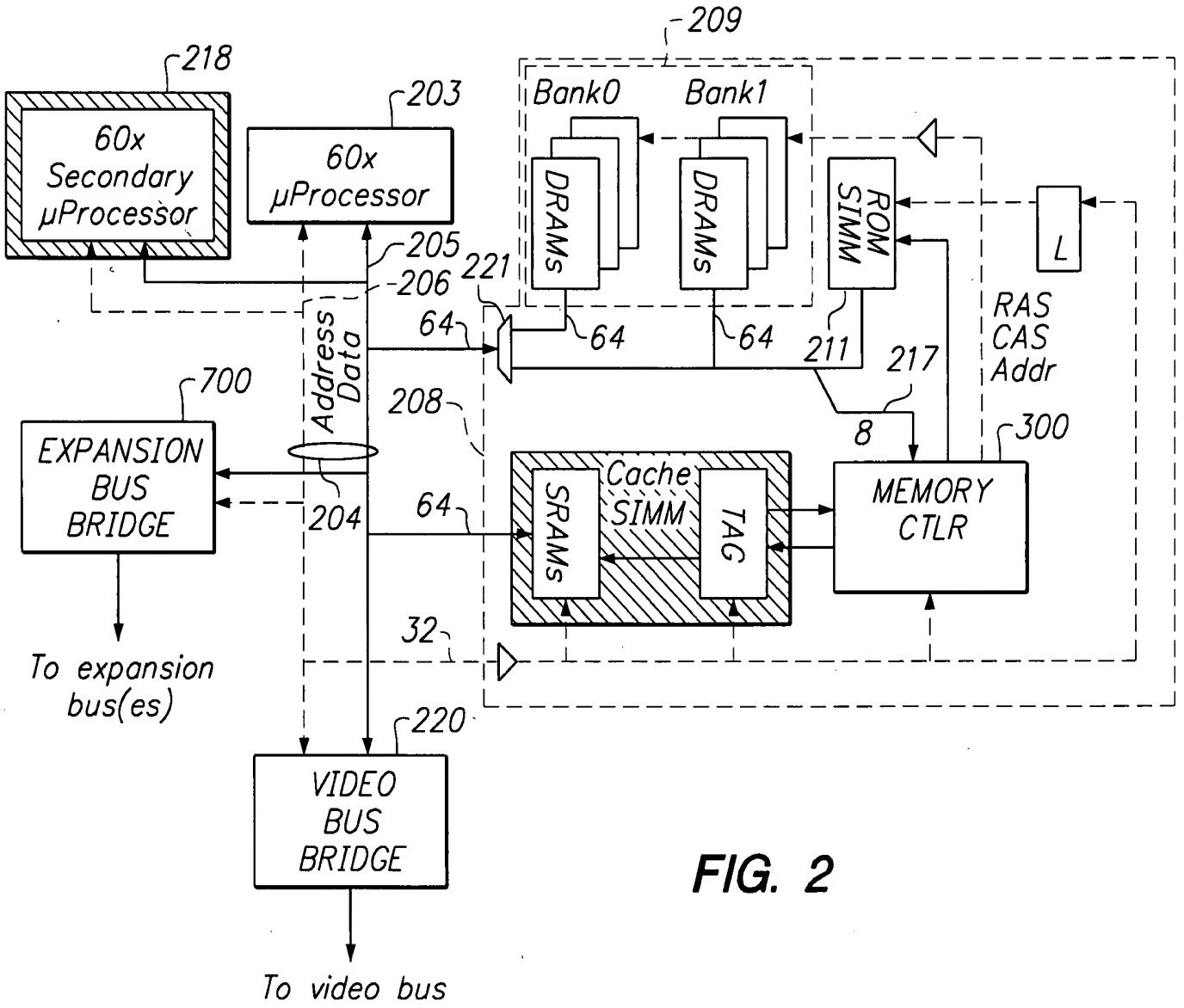

209
218
203
60x
Secondary
µProcessor
60x
µProcessor
Bank0
Bank1
DRAMs
DRAMs
ROM
SIMM
L
205
206
221
64
64
64
211
217
RAS
CAS
Addr
8
700
208
300
Address
Data
EXPANSION
BUS
BRIDGE
204
64
Cache
SIMM
SRAMs
TAG
MEMORY
CTLR
32
To expansion
bus(es)
220
VIDEO
BUS
BRIDGE
To video bus

FIG. 2

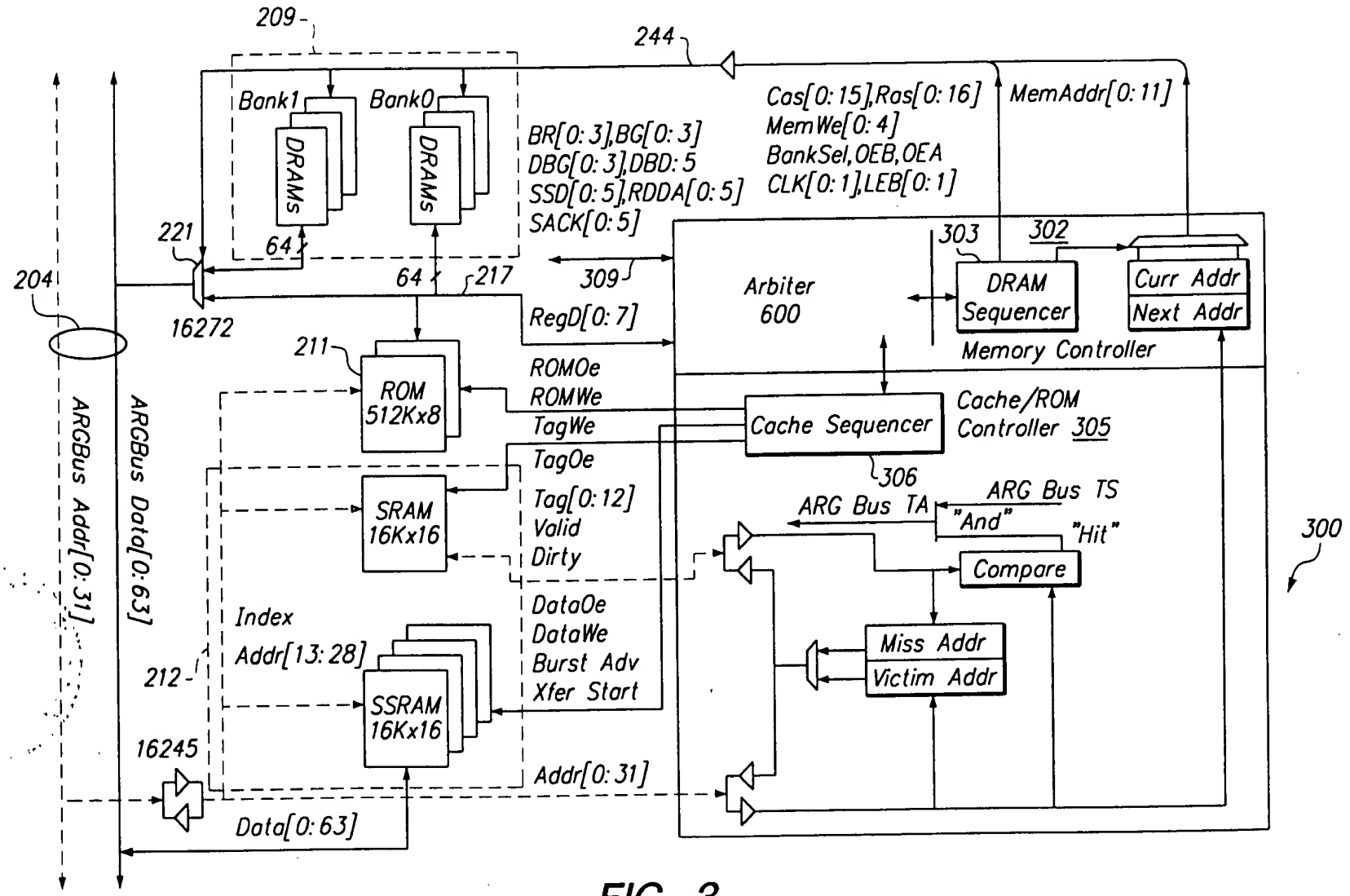

209
244
Bank1
Bank0
DRAMs
DRAMs
BR[0:3],BG[0:3]
DBG[0:3],DBD:5
SSD[0:5],RDDA[0:5]
SACK[0:5]
Cas[0:15],Ras[0:16]
MemWe[0:4]
BankSel,OEB,OEA
CLK[0:1],LEB[0:1]
MemAddr[0:11]
221
64
64
217
309
303
302
204
16272
RegD[0:7]
Arbiter
600
DRAM
Sequencer
Curr Addr
Next Addr
Memory Controller
211
ROM
512Kx8
ROMOe
ROMWe
TagWe
TagOe
Cache Sequencer
Cache/ROM
Controller 305
306
SRAM
16Kx16
Tag[0:12]
Valid
Dirty
ARG Bus TA
ARG Bus TS
"And"
"Hit"
300
Compare
Index
Addr[13:28]
212
SSRAM
16Kx16
DataOe
DataWe
Burst Adv
Xfer Start
Miss Addr
Victim Addr
16245
Addr[0:31]
Data[0:63]
ARGBus Addr[0:31]
ARGBus Data[0:63]

FIG. 3

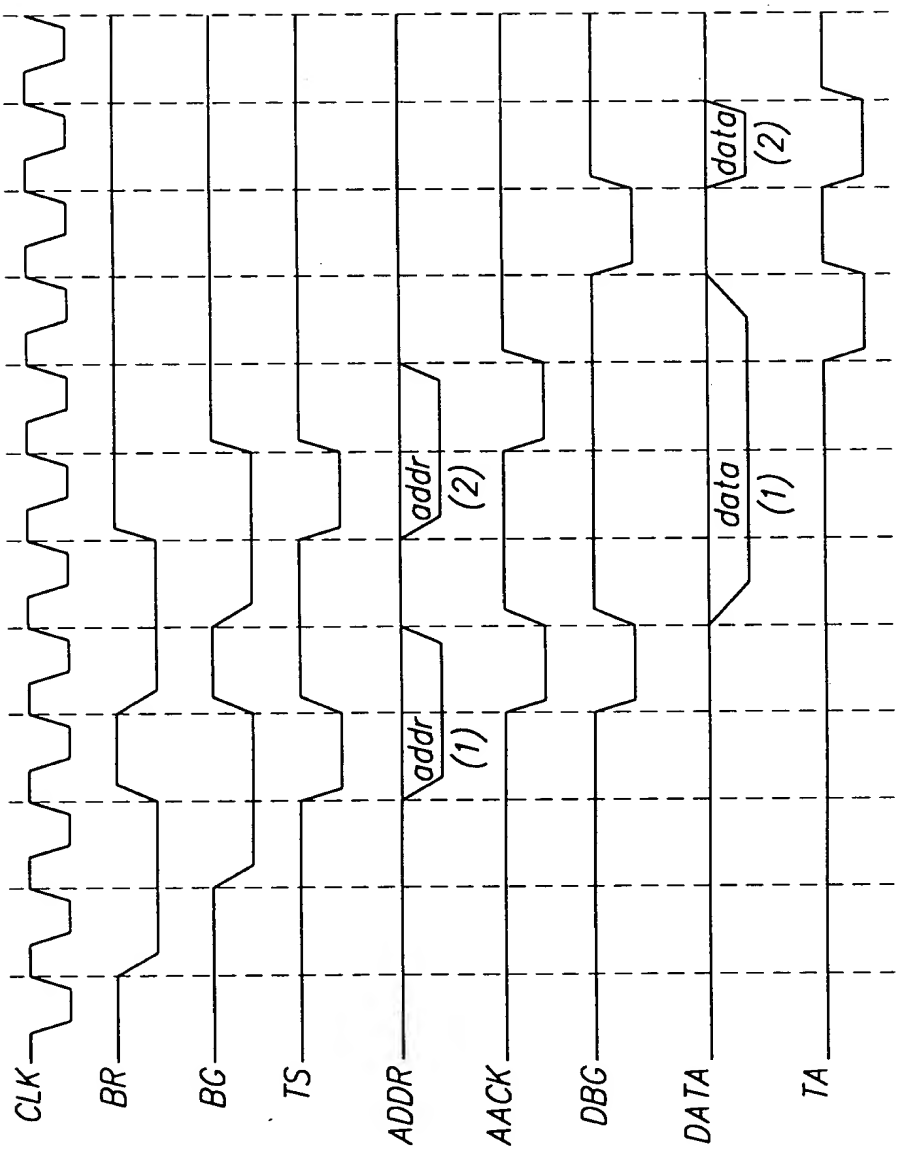


FIG. 4

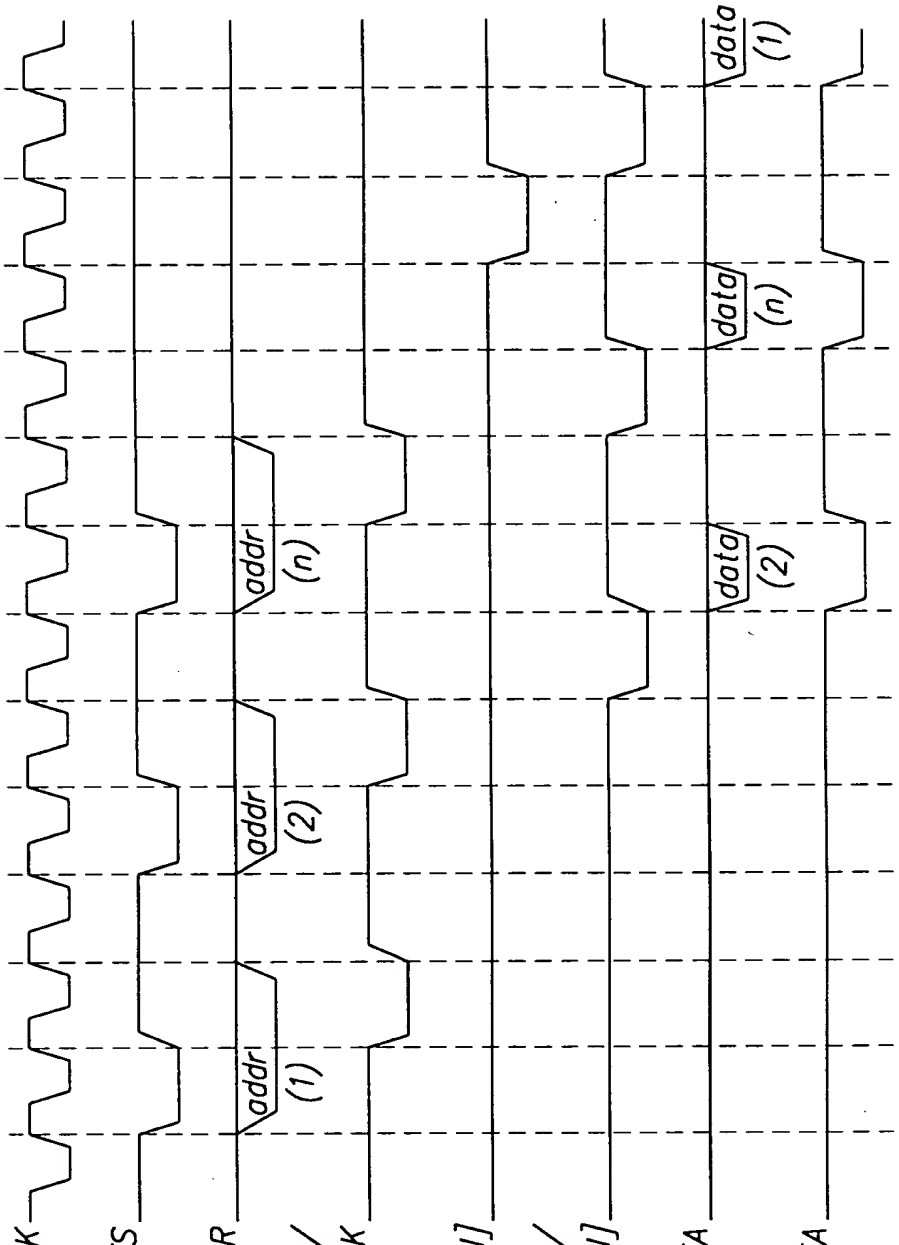

CLK
TS
ADDR
SACK/
AACK
RDDA[N]
DBG[N]/
SSD[N]
DATA
TA
addr
(1)
addr
(2)
addr
(n)
data
(2)
data
(n)
data
(1)

FIG. 5

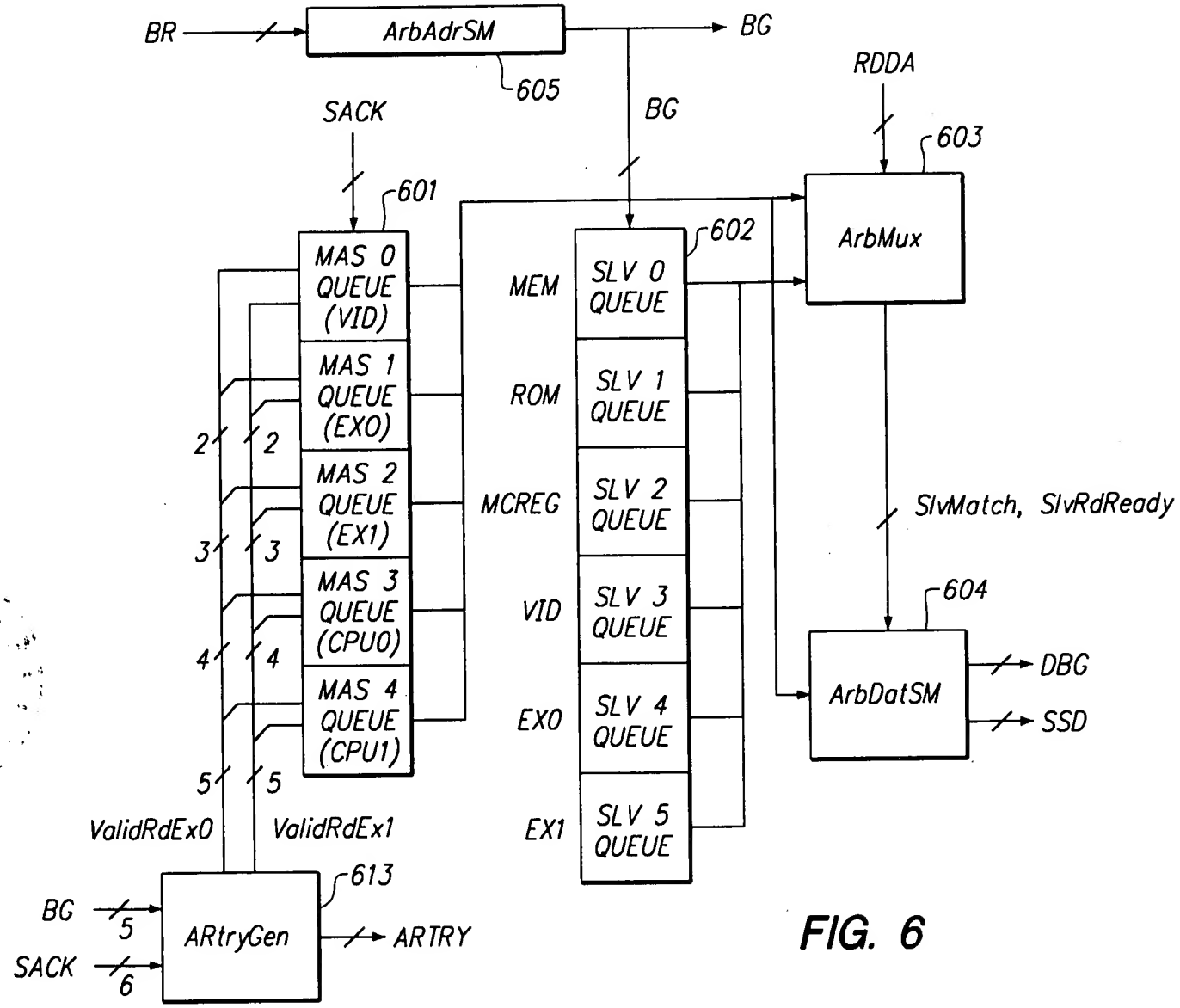

BR
ArbAdrSM
605
BG
RDDA
603
SACK
601
BG
602
ArbMux
MAS 0 QUEUE (VID)
MAS 1 QUEUE (EX0)
MAS 2 QUEUE (EX1)
MAS 3 QUEUE (CPU0)
MAS 4 QUEUE (CPU1)
MEM
ROM
MCREG
VID
EX0
EX1
SLV 0 QUEUE
SLV 1 QUEUE
SLV 2 QUEUE
SLV 3 QUEUE
SLV 4 QUEUE
SLV 5 QUEUE
SlvMatch, SlvRdReady
604
ArbDatSM
DBG
SSD
2
2
3
3
4
4
5
5
ValidRdEx0
ValidRdEx1
613
BG
5
SACK
6
ARtryGen
ARTRY

FIG. 6

FIG. 7

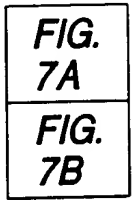
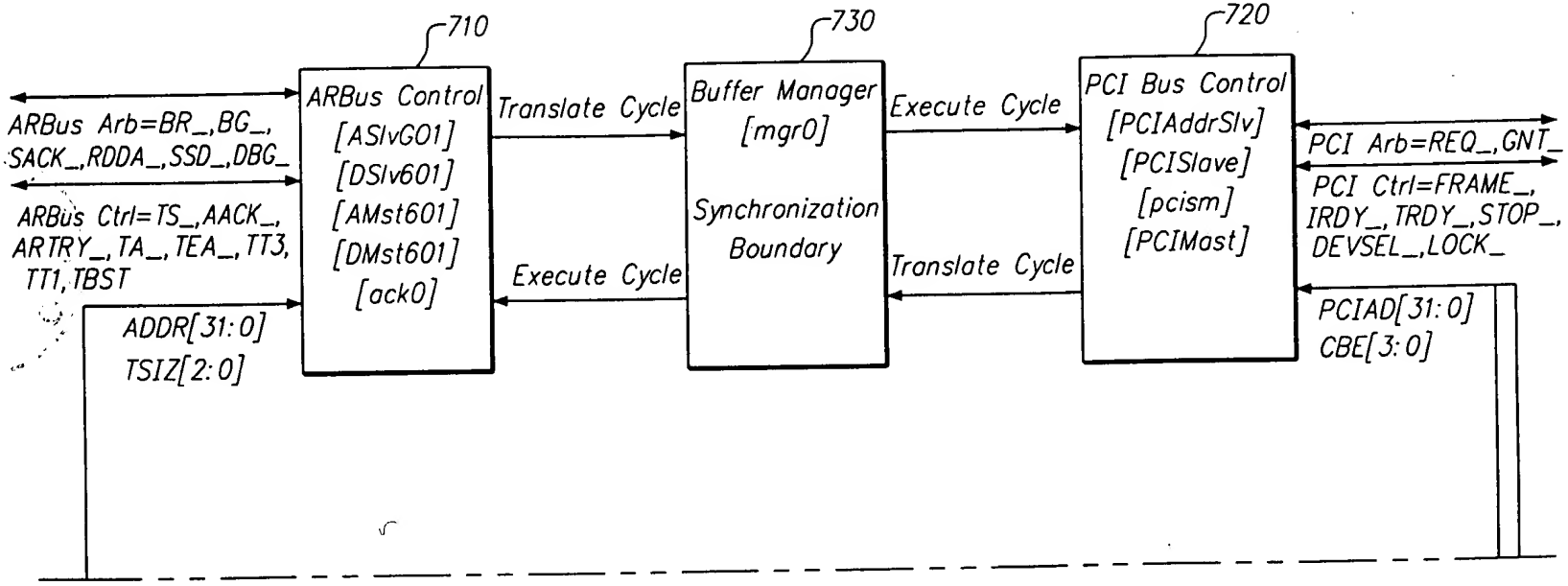


FIG. 7A
FIG. 7B

FIG. 7A


710
730
720
ARBus Control
[ASlvG01]
[DSlv601]
[AMst601]
[DMst601]
[ack0]
Translate Cycle
Execute Cycle
Buffer Manager
[mgr0]
Synchronization
Boundary
Execute Cycle
Translate Cycle
PCI Bus Control
[PCIAddrSlv]
[PCISlave]
[pcism]
[PCIMast]
ARBus Arb=BR_,BG_,
SACK_,RDDA_,SSD_,DBG_
ARBus Ctrl=TS_,AACK_,
ARTRY_,TA_,TEA_,TT3,
TT1,TBST
ADDR[31:0]
TSIZ[2:0]
PCI Arb=REQ_,GNT_
PCI Ctrl=FRAME_,
IRDY_,TRDY_,STOP_,
DEVSEL_,LOCK_
PCIAD[31:0]
CBE[3:0]

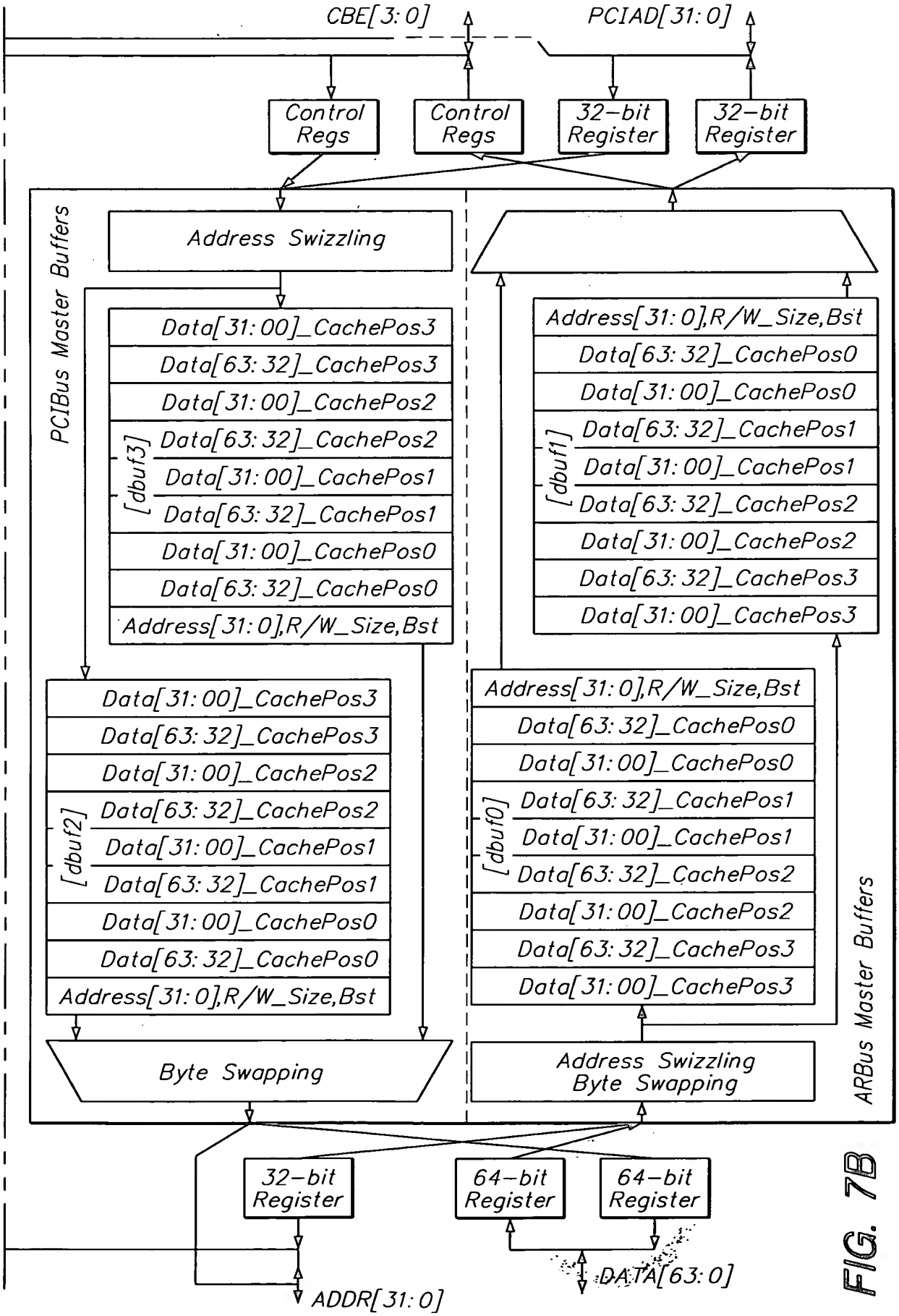

CBE[3:0]
PCIAD[31:0]
Control Regs
Control Regs
32-bit Register
32-bit Register
PCIBus Master Buffers
Address Swizzling
Data[31:00]_CachePos3
Data[63:32]_CachePos3
Data[31:00]_CachePos2
[dbuf3]
Data[63:32]_CachePos2
Data[31:00]_CachePos1
Data[63:32]_CachePos1
Data[31:00]_CachePos0
Data[63:32]_CachePos0
Address[31:0],R/W_Size,Bst
Address[31:0],R/W_Size,Bst
Data[63:32]_CachePos0
Data[31:00]_CachePos0
[dbuf1]
Data[63:32]_CachePos1
Data[31:00]_CachePos1
Data[63:32]_CachePos2
Data[31:00]_CachePos2
Data[63:32]_CachePos3
Data[31:00]_CachePos3
Data[31:00]_CachePos3
Data[63:32]_CachePos3
Data[31:00]_CachePos2
[dbuf2]
Data[63:32]_CachePos2
Data[31:00]_CachePos1
Data[63:32]_CachePos1
Data[31:00]_CachePos0
Data[63:32]_CachePos0
Address[31:0],R/W_Size,Bst
Address[31:0],R/W_Size,Bst
Data[63:32]_CachePos0
Data[31:00]_CachePos0
[dbuf0]
Data[63:32]_CachePos1
Data[31:00]_CachePos1
Data[63:32]_CachePos2
Data[31:00]_CachePos2
Data[63:32]_CachePos3
Data[31:00]_CachePos3
Byte Swapping
Address Swizzling
Byte Swapping
ARBus Master Buffers
32-bit Register
64-bit Register
64-bit Register
ADDR[31:0]
DATA[63:0]

FIG. 7B

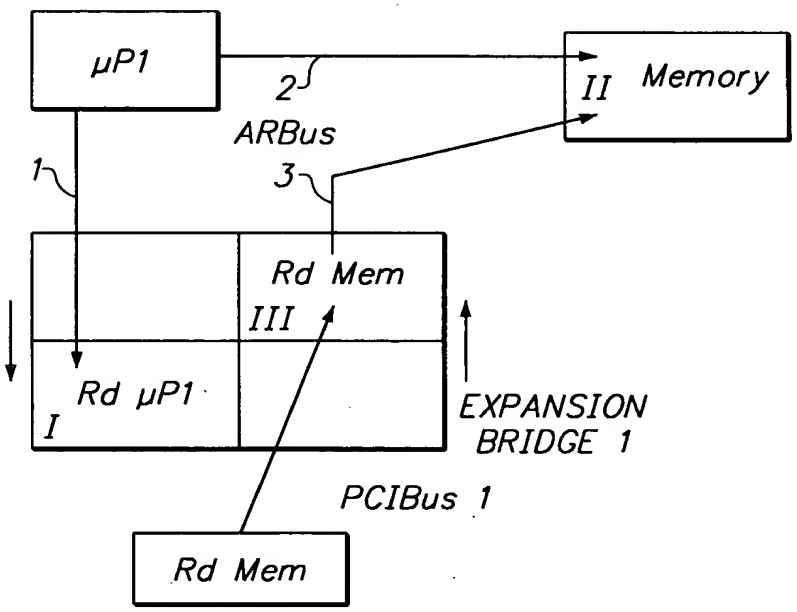

µP1
2
ARBus
II Memory
1
3
Rd Mem
III
Rd µP1
I
EXPANSION
BRIDGE 1
PCIBus 1
Rd Mem

FIG. 8

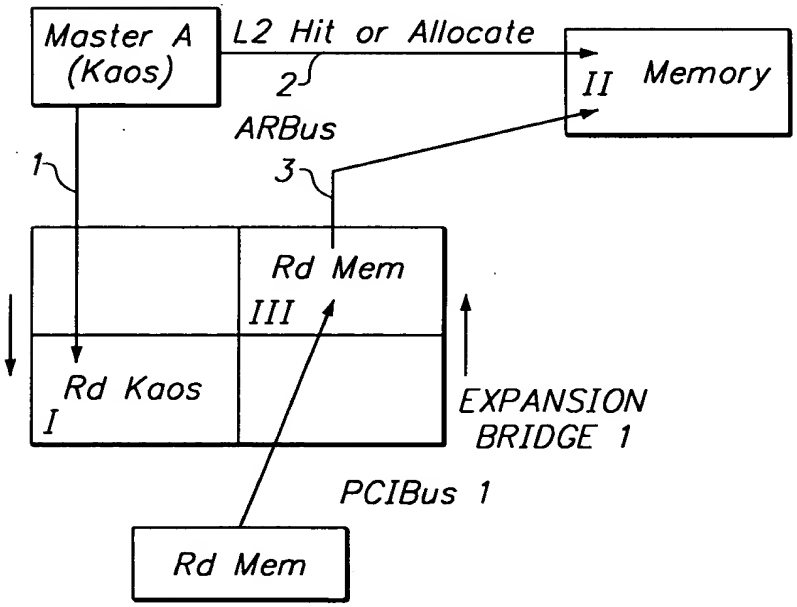

Master A
(Kaos)
L2 Hit or Allocate
2
ARBus
II Memory
1
3
Rd Mem
III
Rd Kaos
I
EXPANSION
BRIDGE 1
PCIBus 1
Rd Mem

FIG. 9

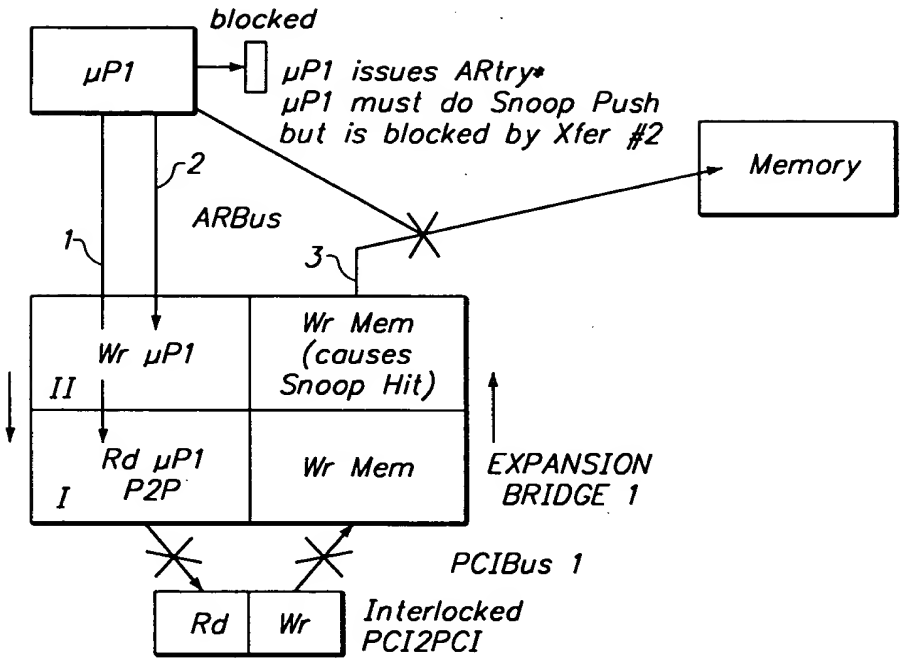

blocked
μP1
μP1 issues ARtry*
μP1 must do Snoop Push
but is blocked by Xfer #2
Memory
2
ARBus
1
3
Wr μP1
II
Wr Mem
(causes
Snoop Hit)
Rd μP1
P2P
I
Wr Mem
EXPANSION
BRIDGE 1
PCIBus 1
Rd
Wr
Interlocked
PCI2PCI

FIG. 10

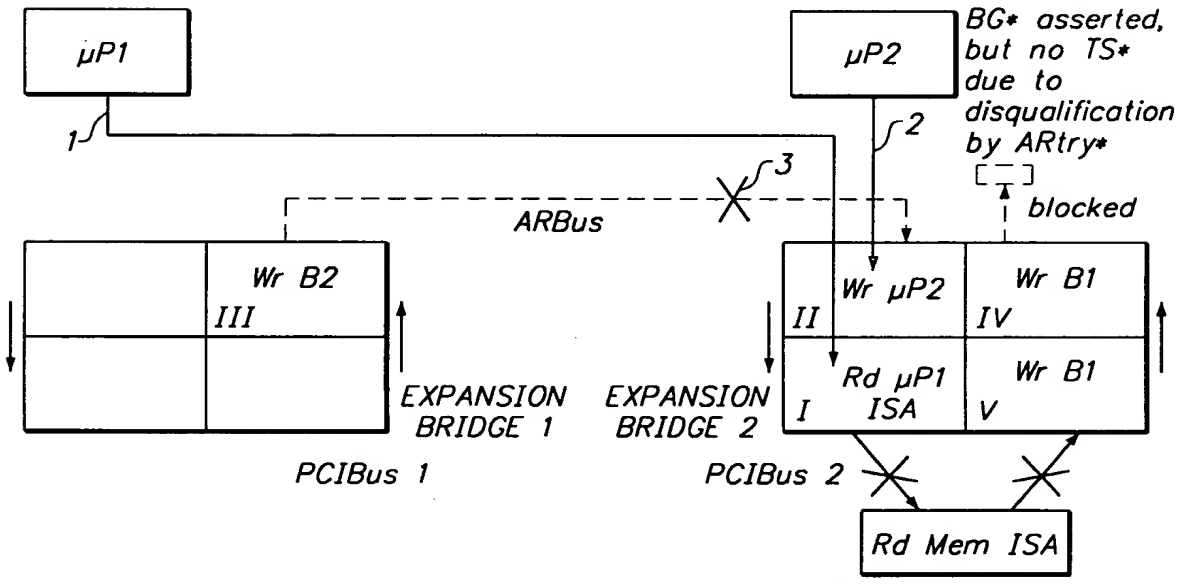

μP1
μP2
BG* asserted,
but no TS*
due to
disqualification
by ARtry*
1
2
3
ARBus
blocked
Wr B2
III
Wr μP2
II
Wr B1
IV
Rd μP1
ISA
I
Wr B1
V
EXPANSION
BRIDGE 1
EXPANSION
BRIDGE 2
PCIBus 1
PCIBus 2
Rd Mem ISA

FIG. 11

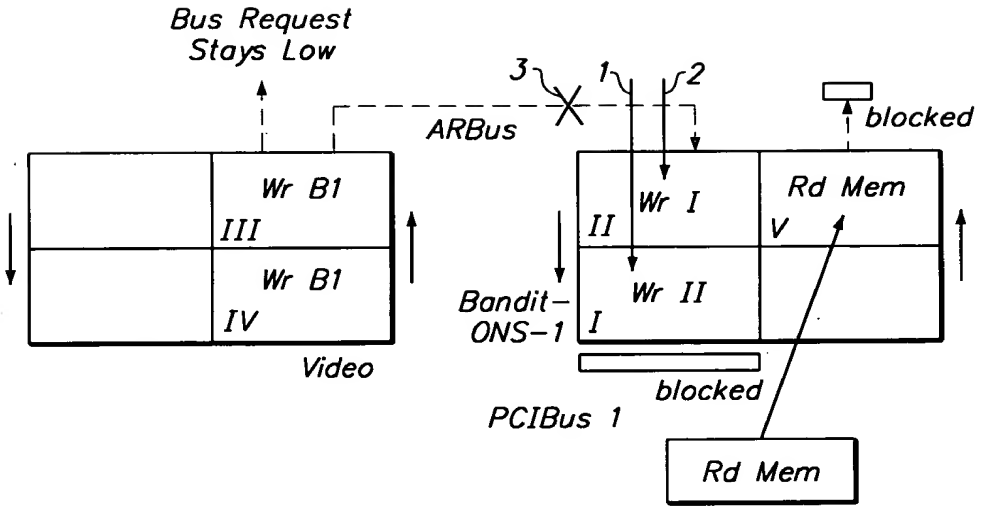

Bus Request
Stays Low
3
1
2
ARBus
blocked
Wr B1
III
Wr B1
IV
Video
Wr I
II
Rd Mem
V
Wr II
I
Bandit–
ONS–1
blocked
PCIBus 1
Rd Mem

FIG. 12

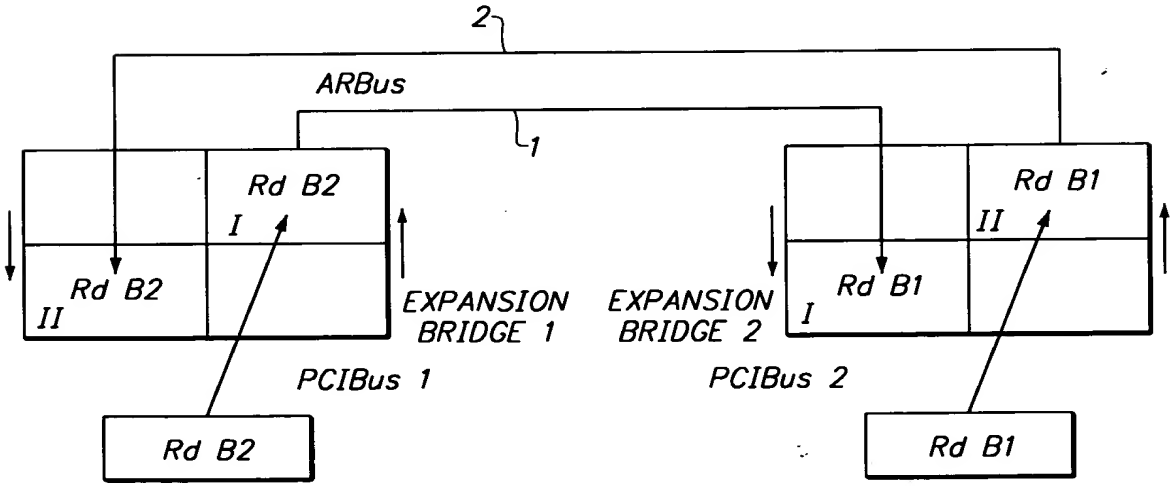

2
ARBus
1
Rd B2
I
Rd B2
II
EXPANSION
BRIDGE 1
PCIBus 1
Rd B2
Rd B1
II
Rd B1
I
EXPANSION
BRIDGE 2
PCIBus 2
Rd B1

FIG. 13

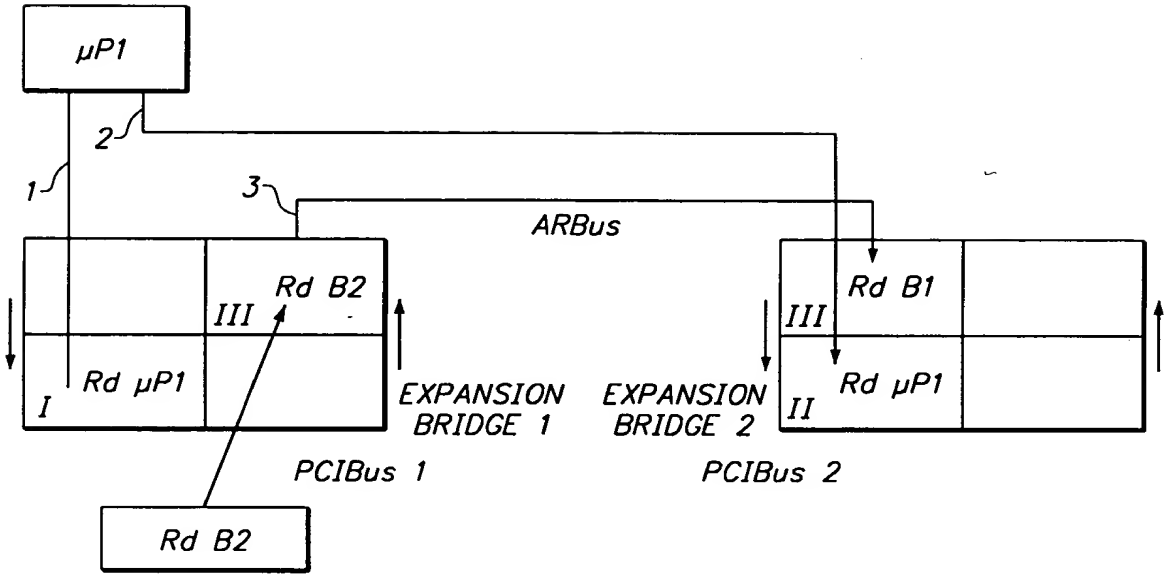

μP1
2
1
3
ARBus
Rd B2
III
Rd B1
III
Rd μP1
I
Rd μP1
II
EXPANSION BRIDGE 1
EXPANSION BRIDGE 2
PCIBus 1
PCIBus 2
Rd B2

FIG. 14

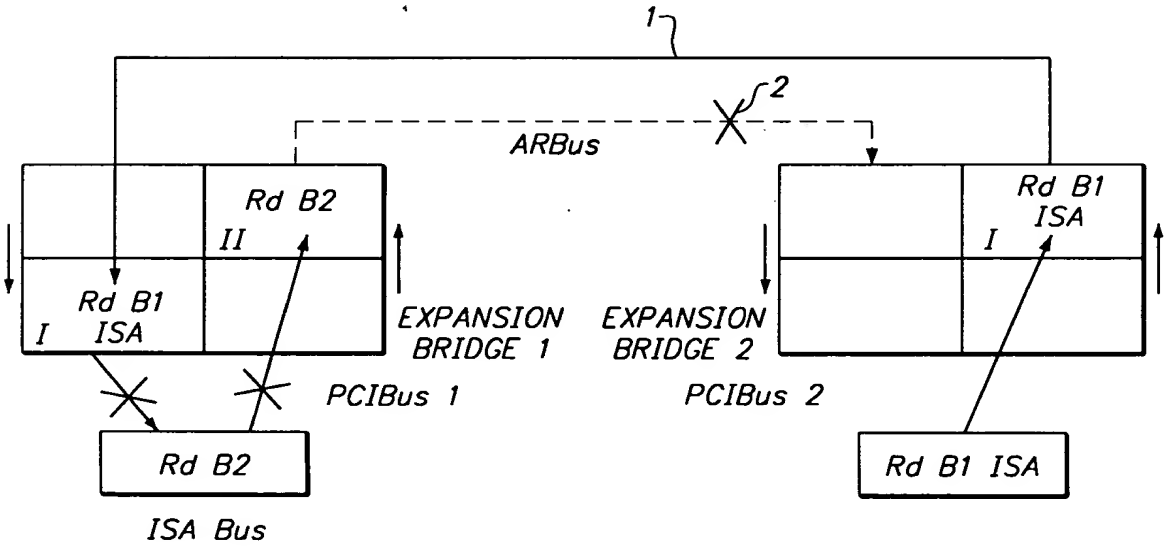

1
2
ARBus
Rd B2
II
Rd B1 ISA
I
Rd B1 ISA
I
EXPANSION BRIDGE 1
EXPANSION BRIDGE 2
PCIBus 1
PCIBus 2
Rd B2
Rd B1 ISA
ISA Bus

FIG. 15

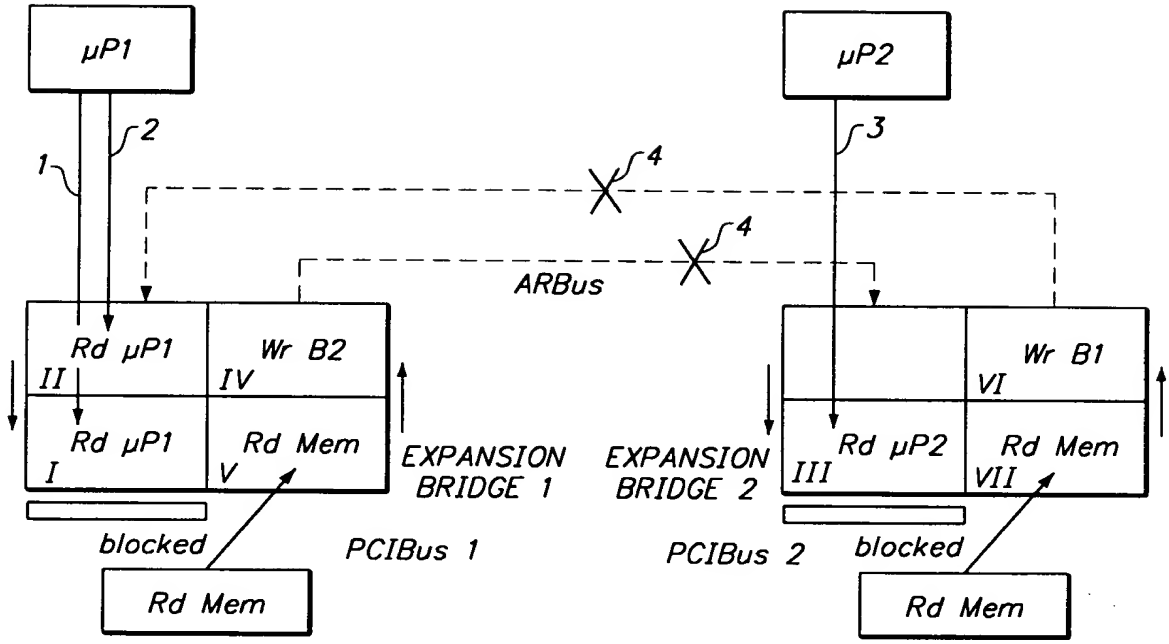

μP1
μP2
1
2
3
4
4
ARBus
Rd μP1
II
Wr B2
IV
Rd μP1
I
Rd Mem
V
EXPANSION BRIDGE 1
EXPANSION BRIDGE 2
Wr B1
VI
Rd μP2
III
Rd Mem
VII
blocked
PCIBus 1
PCIBus 2
blocked
Rd Mem
Rd Mem

FIG. 16

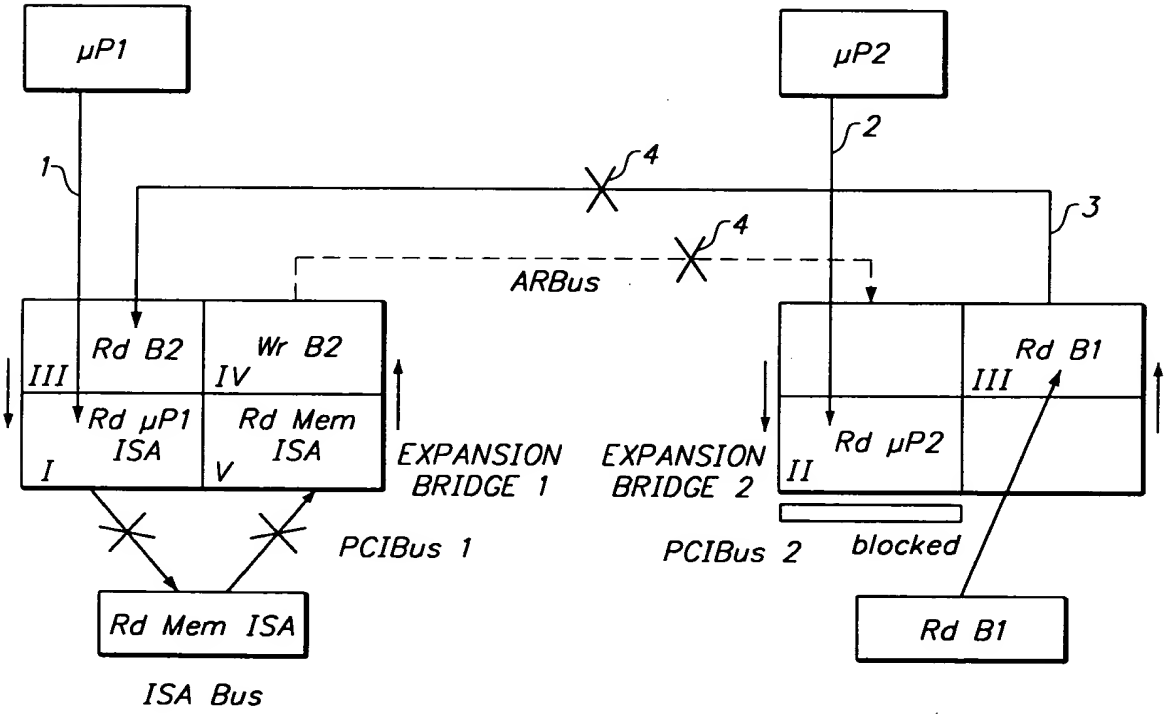

μP1
μP2
1
2
4
3
4
ARBus
III
Rd B2
IV
Wr B2
Rd μP1
ISA
I
Rd Mem
ISA
V
EXPANSION BRIDGE 1
EXPANSION BRIDGE 2
Rd B1
III
Rd μP2
II
PCIBus 1
PCIBus 2
blocked
Rd Mem ISA
Rd B1
ISA Bus

FIG. 17

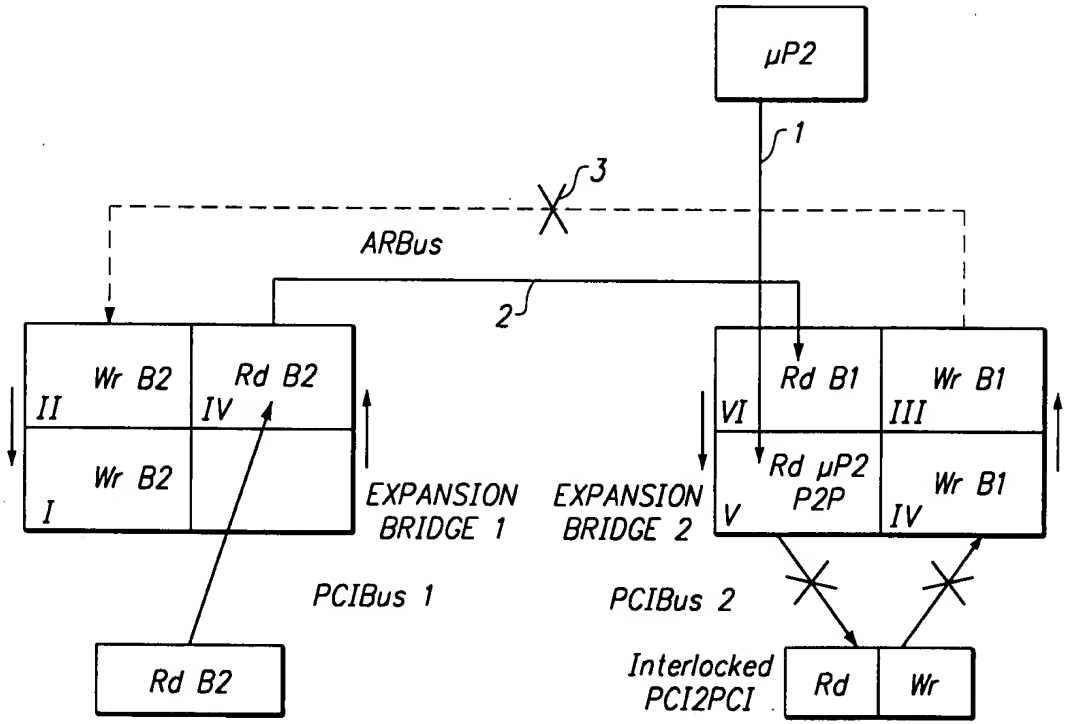

μP2
1
3
ARBus
2
Wr B2
II
Rd B2
IV
Wr B2
I
EXPANSION
BRIDGE 1
EXPANSION
BRIDGE 2
Rd B1
VI
Wr B1
III
Rd μP2
P2P
V
Wr B1
IV
PCIBus 1
PCIBus 2
Rd B2
Interlocked
PCI2PCI
Rd
Wr

FIG. 18

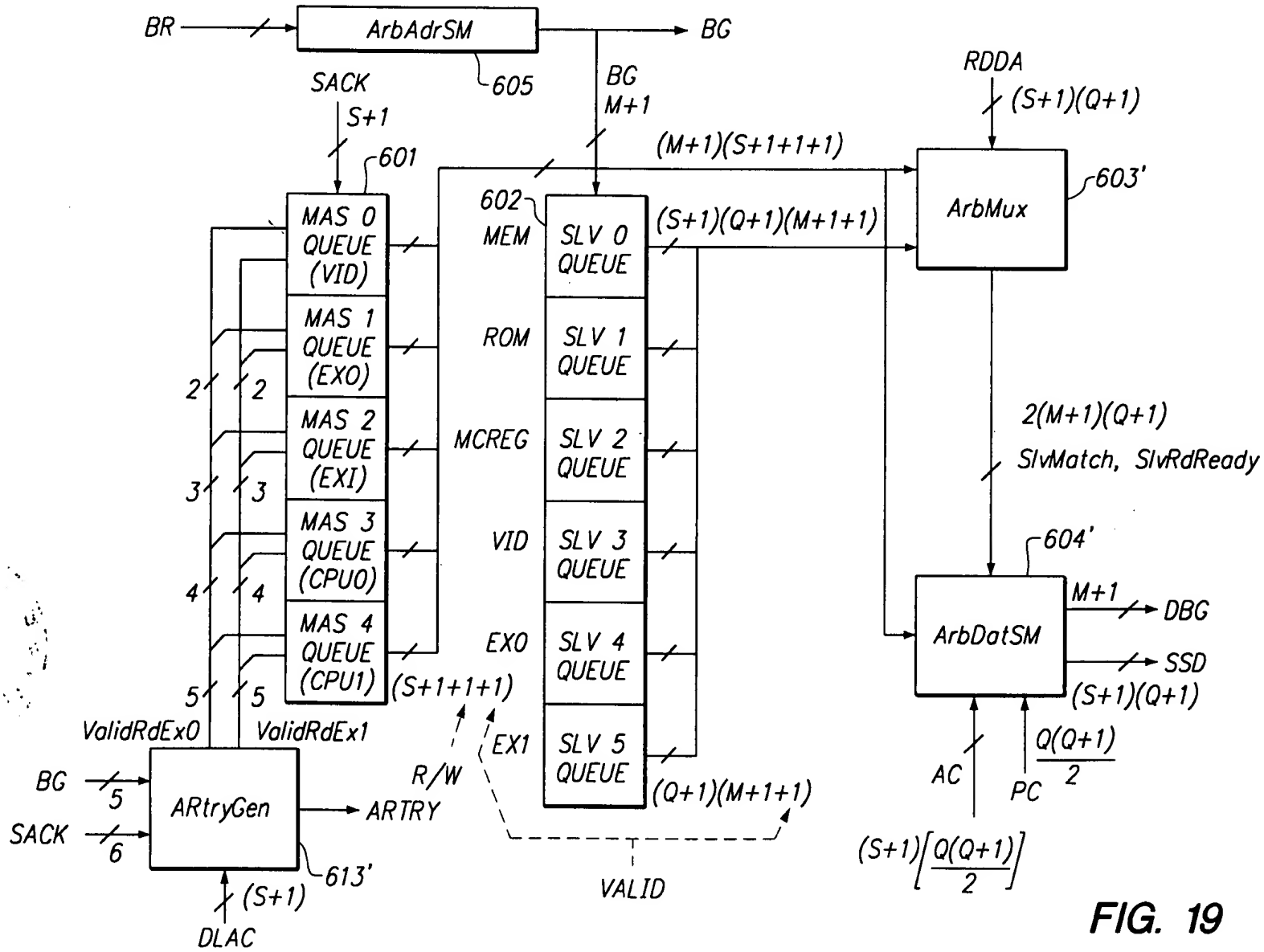

BR
ArbAdrSM
BG
605
SACK
S+1
601
BG
M+1
(M+1)(S+1+1+1)
RDDA
(S+1)(Q+1)
603'
ArbMux
602
MEM
ROM
MCREG
VID
EX0
EX1
MAS 0 QUEUE (VID)
MAS 1 QUEUE (EX0)
MAS 2 QUEUE (EX1)
MAS 3 QUEUE (CPU0)
MAS 4 QUEUE (CPU1)
SLV 0 QUEUE
SLV 1 QUEUE
SLV 2 QUEUE
SLV 3 QUEUE
SLV 4 QUEUE
SLV 5 QUEUE
(S+1)(Q+1)(M+1+1)
(S+1+1+1)
(Q+1)(M+1+1)
2(M+1)(Q+1)
SlvMatch, SlvRdReady
604'
ArbDatSM
M+1
DBG
SSD
(S+1)(Q+1)
AC
PC
Q(Q+1)/2
(S+1)⌈Q(Q+1)/2⌉
ValidRdEx0
ValidRdEx1
BG
SACK
ARtryGen
ARTRY
613'
(S+1)
DLAC
R/W
VALID

FIG. 19

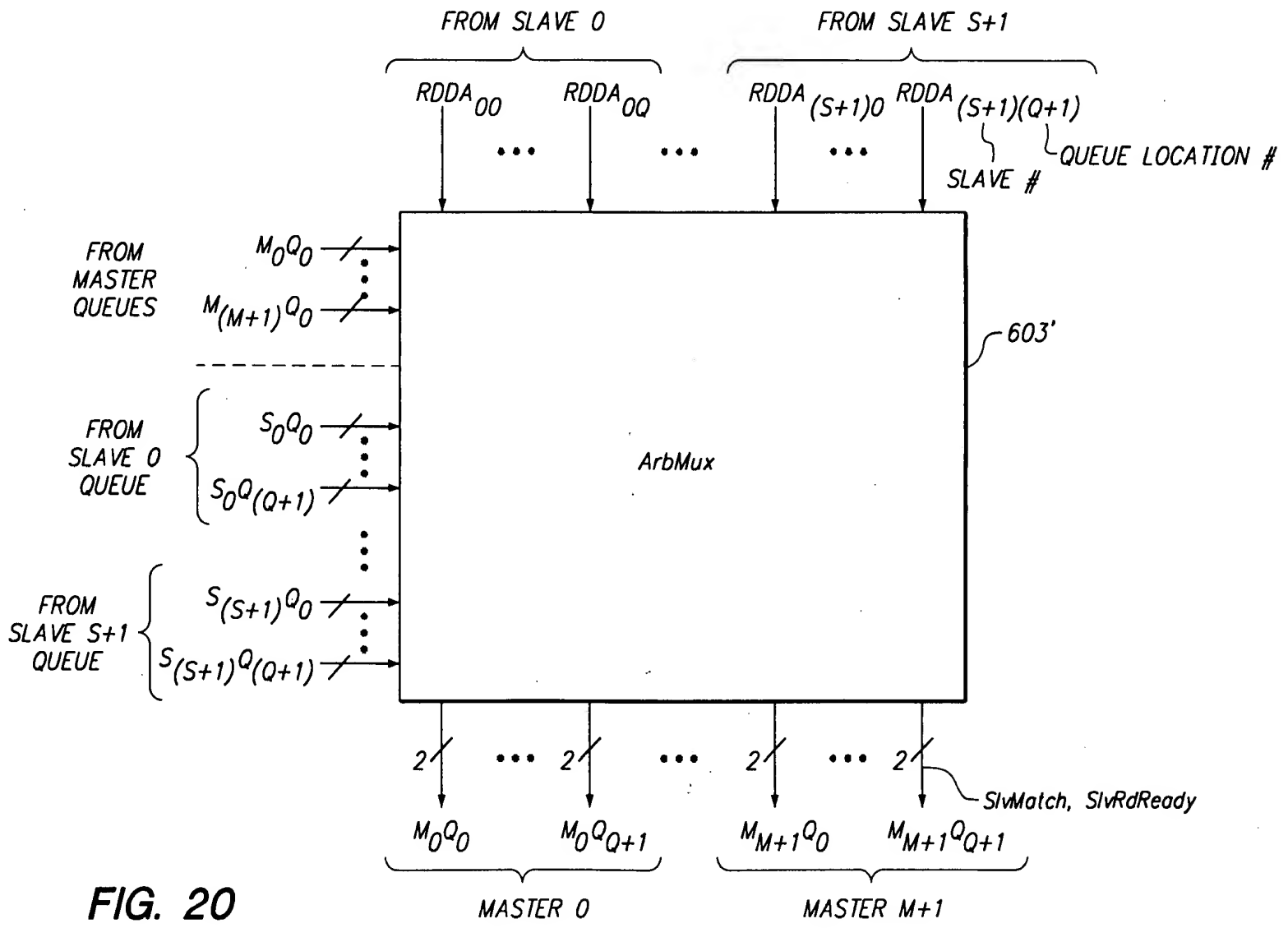

FROM SLAVE 0
FROM SLAVE S+1
RDDA 00
RDDA 0Q
RDDA (S+1)0
RDDA (S+1)(Q+1)
QUEUE LOCATION #
SLAVE #
FROM MASTER QUEUES
M0Q0
M(M+1)Q0
603'
FROM SLAVE 0 QUEUE
S0Q0
S0Q(Q+1)
ArbMux
FROM SLAVE S+1 QUEUE
S(S+1)Q0
S(S+1)Q(Q+1)
2
SlvMatch, SlvRdReady
M0Q0
M0QQ+1
MM+1Q0
MM+1QQ+1
MASTER 0
MASTER M+1

FIG. 20

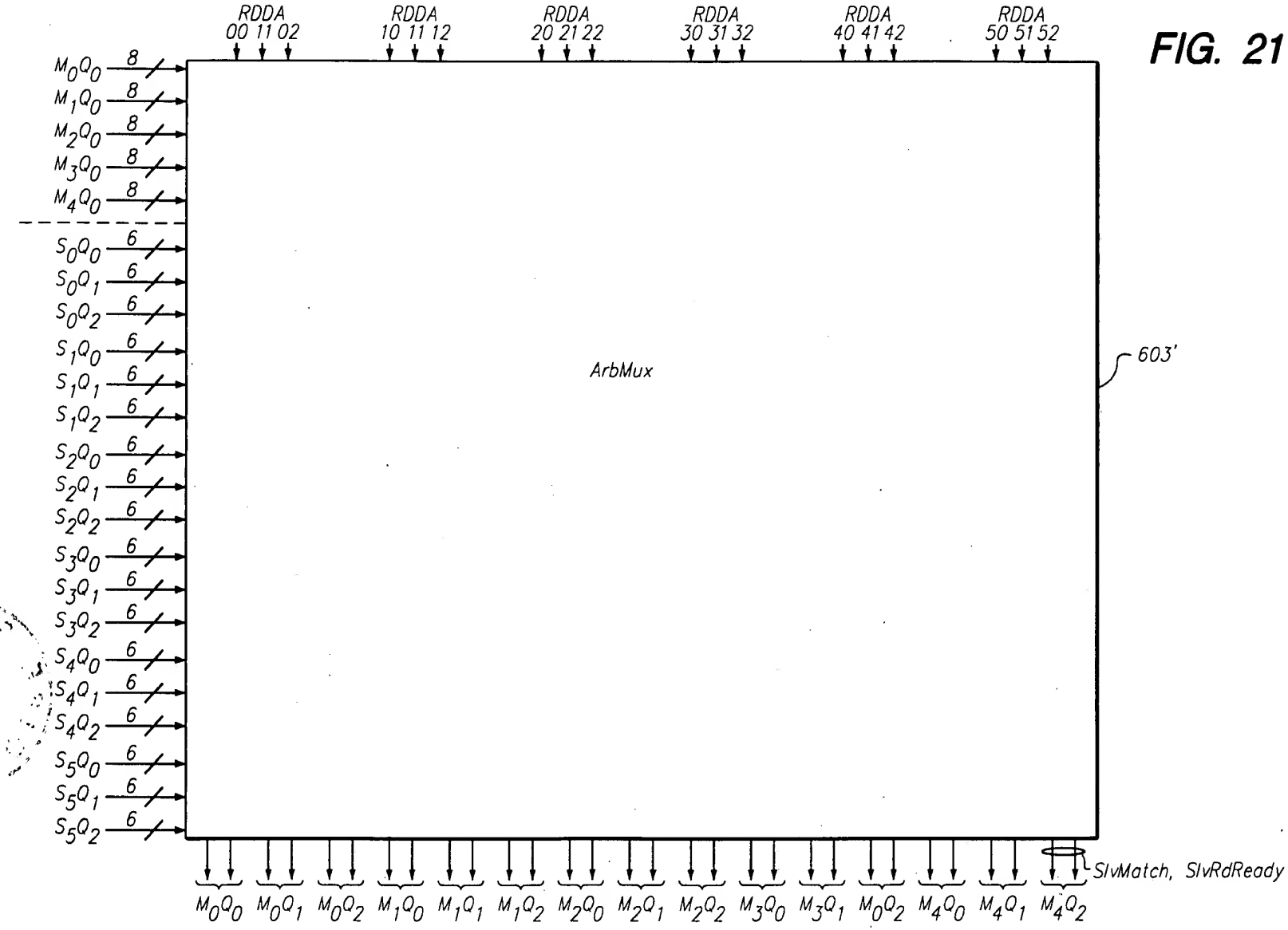

RDDA 00 11 02
RDDA 10 11 12
RDDA 20 21 22
RDDA 30 31 32
RDDA 40 41 42
RDDA 50 51 52
M_0Q_0 8
M_1Q_0 8
M_2Q_0 8
M_3Q_0 8
M_4Q_0 8
S_0Q_0 6
S_0Q_1 6
S_0Q_2 6
S_1Q_0 6
S_1Q_1 6
S_1Q_2 6
S_2Q_0 6
S_2Q_1 6
S_2Q_2 6
S_3Q_0 6
S_3Q_1 6
S_3Q_2 6
S_4Q_0 6
S_4Q_1 6
S_4Q_2 6
S_5Q_0 6
S_5Q_1 6
S_5Q_2 6
ArbMux
603'
M_0Q_0 M_0Q_1 M_0Q_2 M_1Q_0 M_1Q_1 M_1Q_2 M_2Q_0 M_2Q_1 M_2Q_2 M_3Q_0 M_3Q_1 M_0Q_2 M_4Q_0 M_4Q_1 M_4Q_2
SlvMatch, SlvRdReady

FIG. 21

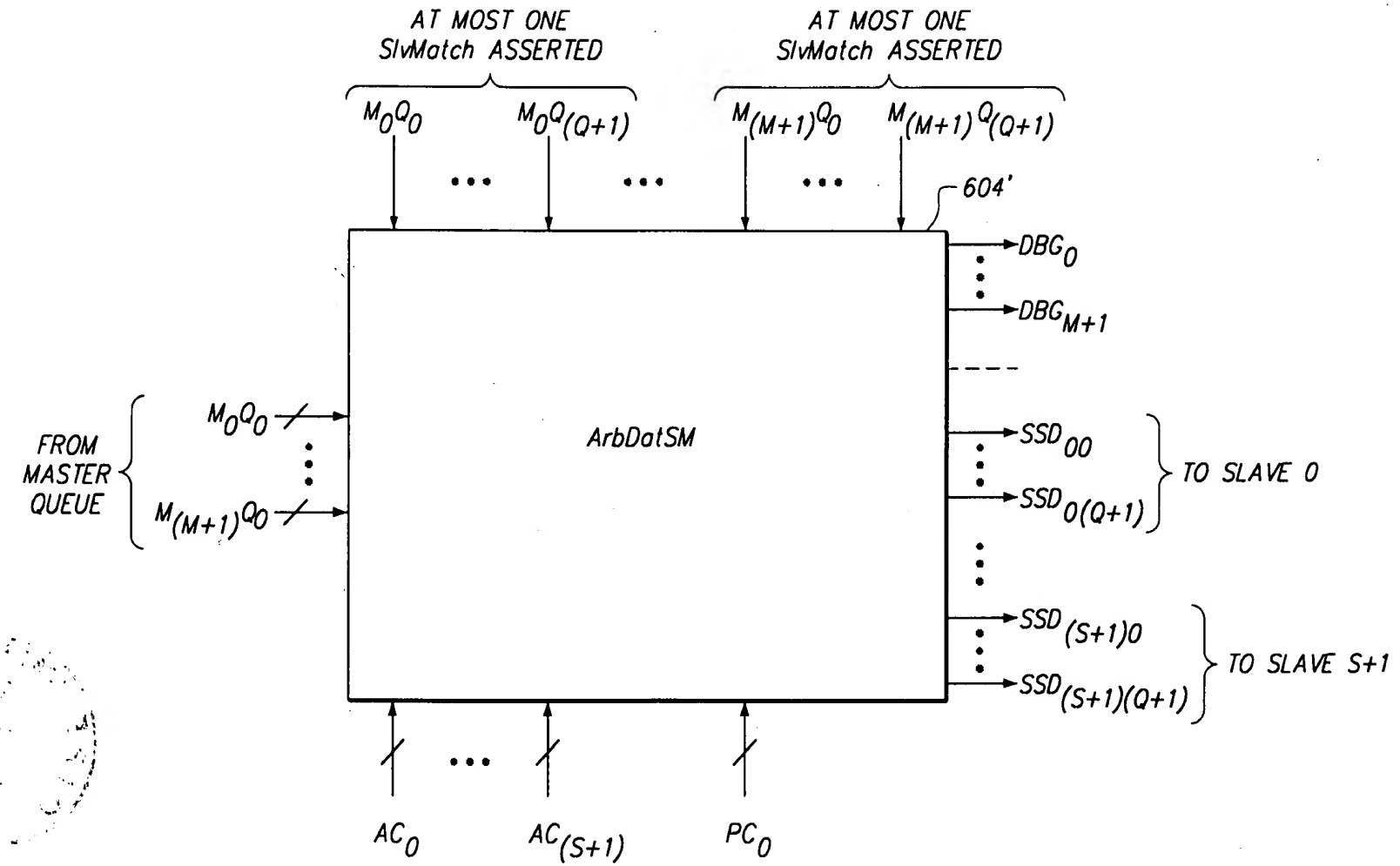

AT MOST ONE SlvMatch ASSERTED
AT MOST ONE SlvMatch ASSERTED
M_0Q_0
$M_0Q_{(Q+1)}$
$M_{(M+1)}Q_0$
$M_{(M+1)}Q_{(Q+1)}$
604'
ArbDatSM
DBG_0
DBG_{M+1}
FROM MASTER QUEUE
M_0Q_0
$M_{(M+1)}Q_0$
SSD_{00}
$SSD_{0(Q+1)}$
TO SLAVE 0
$SSD_{(S+1)0}$
$SSD_{(S+1)(Q+1)}$
TO SLAVE S+1
AC_0
$AC_{(S+1)}$
PC_0

FIG. 22

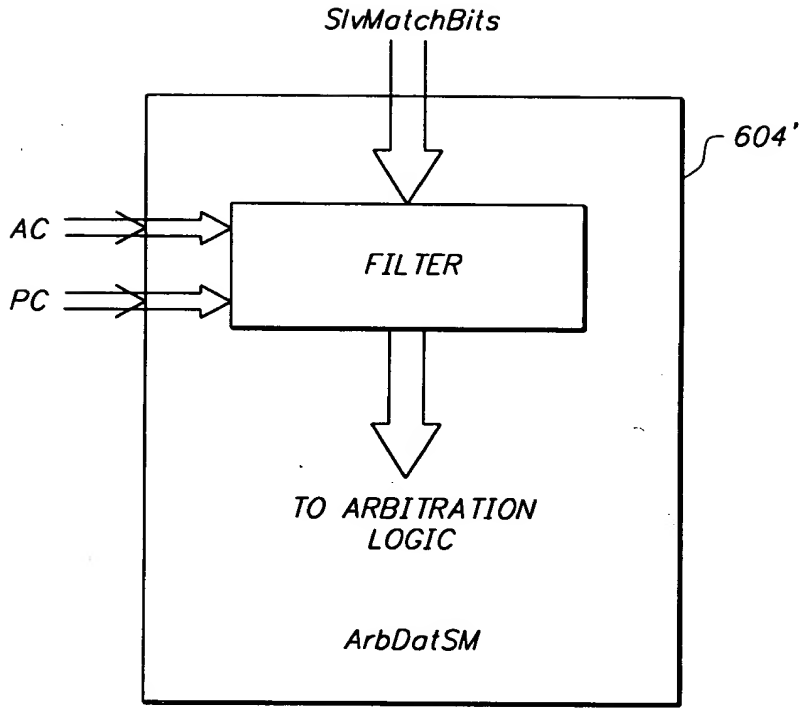

SlvMatchBits
604'
AC
PC
FILTER
TO ARBITRATION LOGIC
ArbDatSM

FIG. 23

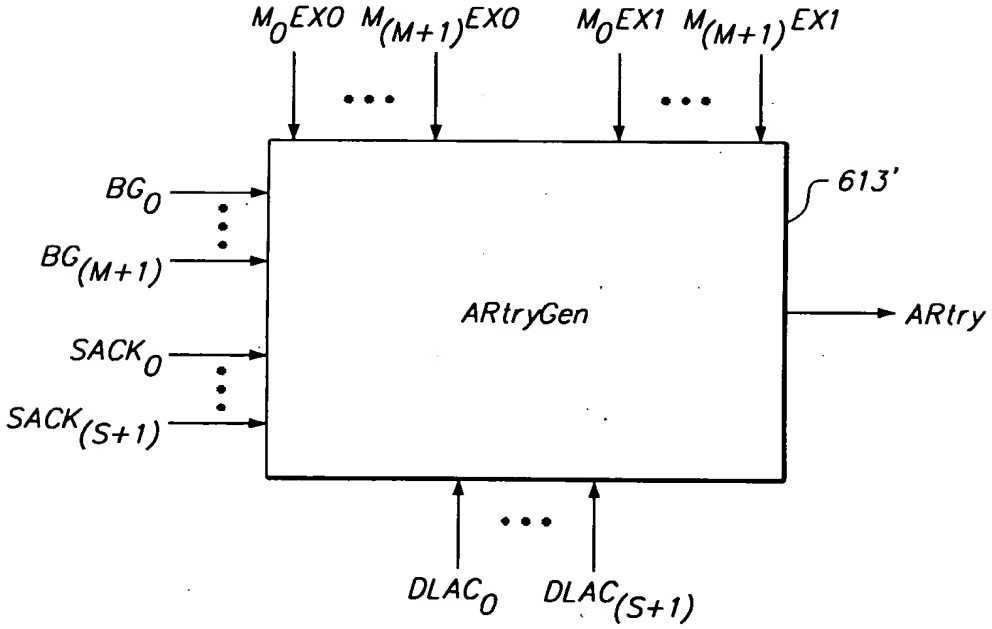

M_0EX0 $M_{(M+1)}EX0$ M_0EX1 $M_{(M+1)}EX1$
613'
BG_0
$BG_{(M+1)}$
$SACK_0$
$SACK_{(S+1)}$
ARtryGen
ARtry
$DLAC_0$ $DLAC_{(S+1)}$

FIG. 25

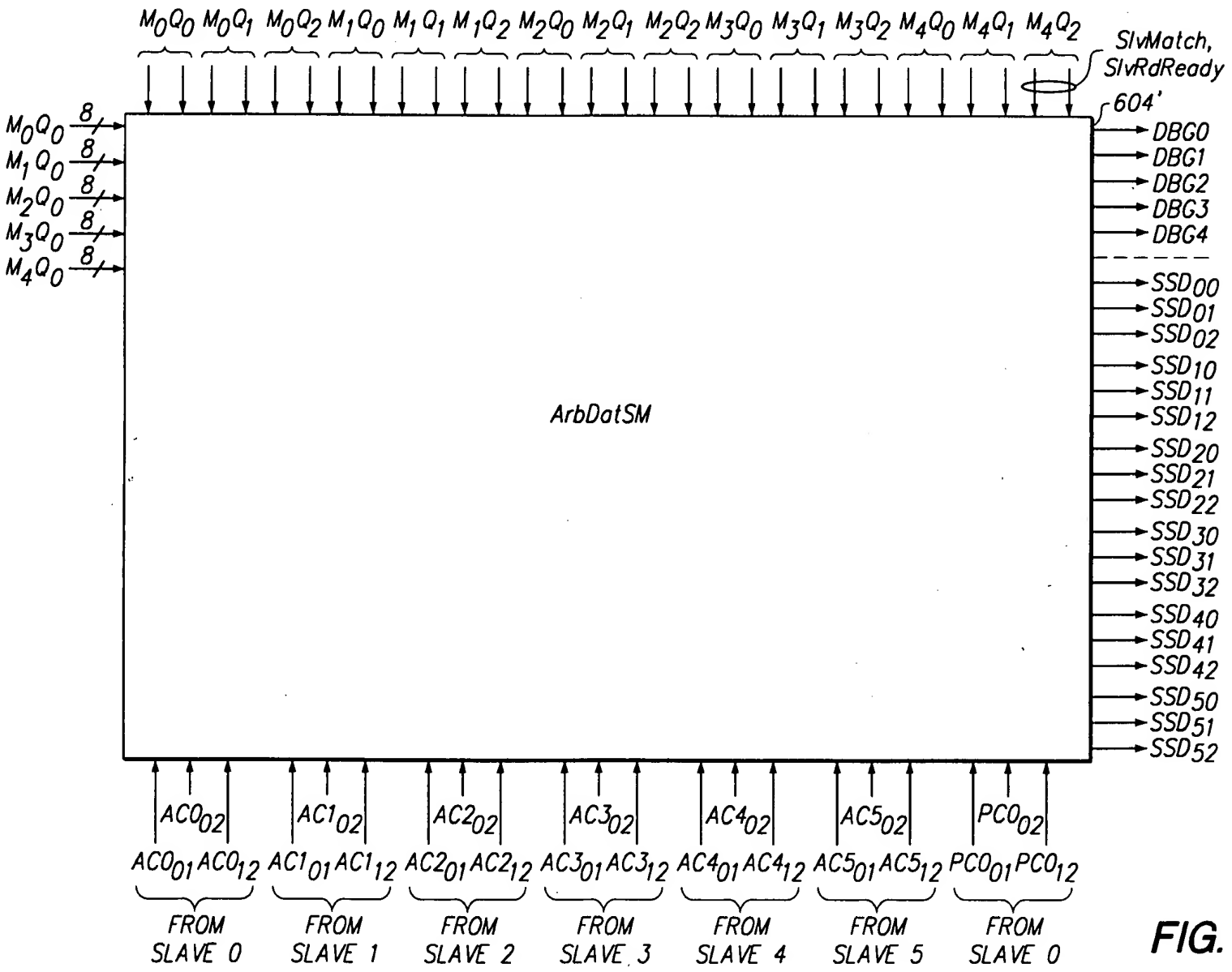

M0Q0 M0Q1 M0Q2 M1Q0 M1Q1 M1Q2 M2Q0 M2Q1 M2Q2 M3Q0 M3Q1 M3Q2 M4Q0 M4Q1 M4Q2
SlvMatch,
SlvRdReady
604'
M0Q0 8
M1Q0 8
M2Q0 8
M3Q0 8
M4Q0 8
ArbDatSM
DBG0
DBG1
DBG2
DBG3
DBG4
SSD00
SSD01
SSD02
SSD10
SSD11
SSD12
SSD20
SSD21
SSD22
SSD30
SSD31
SSD32
SSD40
SSD41
SSD42
SSD50
SSD51
SSD52
AC0 02
AC1 02
AC2 02
AC3 02
AC4 02
AC5 02
PC0 02
AC0 01 AC0 12
AC1 01 AC1 12
AC2 01 AC2 12
AC3 01 AC3 12
AC4 01 AC4 12
AC5 01 AC5 12
PC0 01 PC0 12
FROM SLAVE 0
FROM SLAVE 1
FROM SLAVE 2
FROM SLAVE 3
FROM SLAVE 4
FROM SLAVE 5
FROM SLAVE 0

FIG. 24

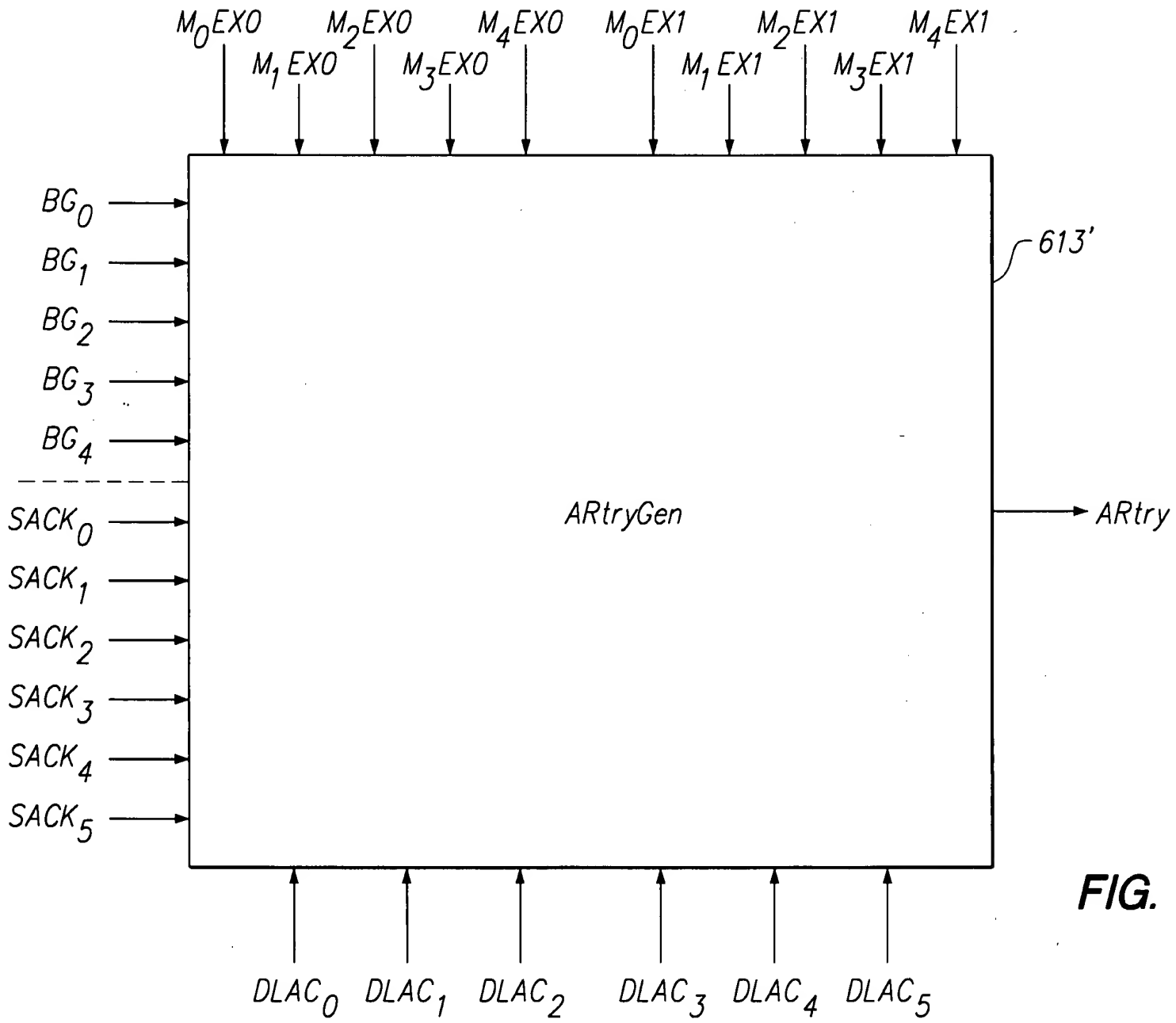

M_0EX0
M_1EX0
M_2EX0
M_3EX0
M_4EX0
M_0EX1
M_1EX1
M_2EX1
M_3EX1
M_4EX1
BG_0
BG_1
BG_2
BG_3
BG_4
$SACK_0$
$SACK_1$
$SACK_2$
$SACK_3$
$SACK_4$
$SACK_5$
ARtryGen
613'
ARtry
$DLAC_0$
$DLAC_1$
$DLAC_2$
$DLAC_3$
$DLAC_4$
$DLAC_5$

FIG. 26